ABSTRACT OF THE DISCLOSURE

A bus that may be used in an integrated circuit chip. The bus generally comprises a master interface, a slave interface, and a control logic. The master interface may be configured to (i) receive an early command signal having a predetermined timing relationship to a first clock edge and (ii) present a bus wait signal proximate a second clock edge. The slave interface may be configured to (i) present a command signal a delay after the first clock edge and (ii) receive a slave wait signal. The control logic may be configured to (i) register the early command signal to generate the command signal and (ii) convert the slave wait signal into the bus wait signal.